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Application No.: 10/680,209

Docket No.: 4459-133

REMARKS

Applicants appreciate the Examiner's thorough review of the present application, and respectfully request reconsideration in light of the preceding amendments and the following remarks.

Claims 1-21 are pending in the application. Independent claims 1 and 14 have been amended to better define the claimed invention. Claims 2-3 and 15-16 have been amended to be consistent with the amended language of claim 1. Claim 21 has been added to provide Applicants with the scope of protection to which they are believed entitled. The amended/new claims find solid support in the original specification and drawings. No new matter has been introduced through the foregoing amendments.

The 35 U.S.C. 102 rejection of claims 1, 8, 14-15, and 17-20 as being anticipated by *Centola et al.* (U.S. Patent No. 6,633,490) is traversed because the applied reference clearly fails to teach or disclose each and every element of the rejected claims.

With regard to Claim 1:

The Examiner mischaracterized the male connector (110-1, 2) disclosed by *Centola et al.* as the external electronic device recited in the claim. It is the backplane board (100) of *Centola et al.* that appears to be similar to the external electronic device recited in the claim. In col. 4, lines 42-46 and FIG.5 of *Centola et al.*, it is disclosed that the male connector (110-1, 2) of *Centola et al.* is part of the backplane board (100). Thus, the male connector (110-1, 2) of *Centola et al.* cannot be regarded as an external electronic device; it can be regarded, at best, only as part of the "external electronic device" or backplane board 100. Therefore, *Centola et al.* teach, at best, only an "external electronic device" or backplane board 100, and clearly fail to disclose the relationship between the external printed wiring board and the substrate as recited

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in the claim.

Notwithstanding, the above, claim 1 has been amended to specifically define over *Centola et al.*

Amended claim 1 now recites a package for electrically connecting to an external printed wiring board and an external electronic device comprising: a substrate having a first surface for electrically connecting to the external printed wiring board, and a second surface opposite to the first surface; a semiconductor chip disposed on and electrically connected to the substrate; and a connector disposed on the second, opposite surface of the substrate for electrically connecting the semiconductor chip to the external electronic device.

The claimed invention finds support in FIGS. 1 and 2 of the instant application and has the following advantages. In particular, the substrate (16, 36) has a lower (first) surface which is exposed out of the semiconductor packages (10, 30). Moreover, the first surface of the substrate (16, 36) is used for electrical connection to the first external printed wiring board (24) in a first direction, and the connector (22, 42) is disposed on an upper (second) surface of the substrate for electrical connection to an external electronic device or a second external printed wiring board in a second direction. Thus, the disclosed semiconductor package can be electrically connected to different external printed wiring board(s) and electronic device(s) in different directions.

Centola et al. do not appear to fairly teach or disclose the claimed invention and the disclosed advantages.

On page 2, paragraph 3 of the Office Action, the Examiner alleged that *Centola et al.* disclose a package for electrically connecting to an external printed wiring board (100) and an external electronic device (110-1, 2), the package comprising: a substrate (105-1) electrically connected to the external printed wiring board (100); a semiconductor chip (400) disposed on and electrically connected to the substrate (105-1); and a connector (115-1) disposed on the

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substrate (105-1) for electrically connecting the semiconductor chip (400) to the external electronic device (110-1, 2), i.e., the disclosure in FIGS. 3(a)-5 of *Centola et al.* However, the first printed circuit board (105-1) of *Centola et al.* has a lower surface (adjacent 300 in FIG 4) which cannot be exposed out of the electronic board assembly because the insulative layer (300) is attached to that surface of the first printed circuit board (105-1). Thus, **Centola et al. fail to disclose a substrate having a lower (first) surface which is exposed out of the semiconductor packages and is used for electrical connection to an external printed wiring board in a first direction.** Moreover, *Centola et al.* only disclose that the connector (115-1) is electrically connected to the male connector (110-1, 2) of the backplane board (100) **in a single direction**, e.g., as shown in FIGS. 1-3 and 5-6 of *Centola et al.* Thus, **Centola et al. would fail to achieve the advantage of the claimed invention that the semiconductor package can be electrically connected to different external printed wiring board(s) and electronic device(s) in different directions.**

Accordingly, amended claim 1 is not anticipated by and is clearly patentable over *Centola et al.*

With regard to Claim 8:

The Examiner mischaracterized the insulative layer (300) disclosed by *Centola et al.* as the medium substrate recited in the claim. The insulative layer (300) of *Centola et al.* is not a kind of medium substrate. Thus, **Centola et al. fail to disclose the relationship among the medium substrate, the first substrate and the second substrate**, as recited in the claim.

In addition, claim 8 recites a package for electrically connecting to an external printed wiring board and an external electronic device, comprising: a first substrate; a first semiconductor chip electrically connected to the first substrate; a second substrate; a second semiconductor chip electrically connected to the second substrate; **a medium substrate electrically connected to the first substrate and the second substrate**; and **a connector**

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electrically connected to the first substrate and the second substrate, wherein the first substrate is electrically connected to the external printed wiring board and the connector is electrically connected to the external electronic device.

The claimed invention finds support in FIG. 4 of the instant application and has the following advantages. In particular, the medium substrate 68 is electrically connected to the first substrate 56 and the second substrate 58, and the connector 70 is electrically connected to the first substrate 56 and the second substrate 58. The insulative layer (300) of *Centola et al.* is not a kind of medium substrate. Thus, *Centola et al.* fail to disclose the claimed medium substrate that is electrically connected to the first substrate and the second substrate. Furthermore, the connector (115-1) of *Centola et al.* cannot be electrically connected to the first printed circuit board (105-1) and the second printed circuit board (105-2) simultaneously. Thus, *Centola et al.* fail to disclose the claimed connector that is electrically connected to the first substrate and the second substrate.

Accordingly, claim 8 is not anticipated by and is clearly patentable over *Centola et al.*

With regard to Claim 14:

Amended claim 14 now recites a semiconductor package for electrically connecting to an external electronic device, comprising: a substrate having opposite upper and lower surfaces, wherein the lower surface is oriented in a first direction; a semiconductor chip disposed on and electrically connected to the upper surface of the substrate; and a connector disposed on the upper surface of the substrate for electrically connecting the semiconductor chip to the external electronic device in a second direction different from the first direction.

The claimed invention finds support in FIGS. 1 and 2 of the instant application and has the following advantages. In particular, the semiconductor packages (10, 30) include the substrate (16, 36) having a lower surface which is oriented in a first (e.g., downward) direction.

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The lower surface of the substrate (16, 36) can be electrically connected to an external printed wiring board in the first (e.g., downward) direction, and the connector (22, 42) disposed on the upper surface can be electrically connected to an external electronic device or a second external printed wiring board in a second (e.g., upward (FIG. 1) or sideward (FIG. 2)) direction. Thus, the claimed semiconductor package can be electrically connected to different external printed wiring board(s) and electronic device(s) in different directions.

However, *Centola et al.* only disclose the connector (115-1) being electrically connected to the male connector (110-1, 2) of the backplane board (100) in a single direction, e.g., as shown in FIGS. 1-3 and 5-6 of the reference. Thus, *Centola et al.* would fail to achieve the advantage of the claimed invention that the semiconductor package can be electrically connected to different external printed wiring board(s) and electronic device(s) in different directions.

Accordingly, amended claim 14 is not anticipated by and is clearly patentable over *Centola et al.*

With regard to Claim 15:

The Examiner mischaracterized the mechanical maintaining means (500) disclosed by *Centola et al.* as the claimed conductive elements. The mechanical maintaining means (500) of *Centola et al.* is used for mechanically maintaining the first printed circuit board (105-1), the insulative layer (300) and the second printed circuit board (105-2), and is not a kind of conductive element. See column 4, lines 61-65 of *Centola et al.* Thus, *Centola et al.* fail to disclose the claimed lower conductive element, e.g., solder ball, on the lower surface of the substrate for electrically connecting the chip to the external printed wiring board.

In addition, there is no teaching in *Centola et al.* that the screws or rivets 500 electrically connect the chip to the external printed wiring board as presently claimed. Mechanical

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maintaining means, such as screws or rivets, are simply not configured to transmit electrical signals.

Accordingly, claim 15 is not anticipated by and is clearly patentable over *Centola et al.*

Furthermore, claim 15 depends from claim 1, and is considered patentable at least for the reasons advanced with respect to claim 1.

With regard to Claims 17 and 20:

Claim 17 depends from claim 1, and is considered patentable at least for the reasons advanced with respect to claim 1.

Claim 20 depends from claim 8, and is considered patentable at least for the reasons advanced with respect to claim 8.

With regard to Claim 18:

Claim 18 depends from claim 8, and is considered patentable at least for the reasons advanced with respect to claim 8.

In addition, the applied reference clearly fails to teach or disclose the invention of claim 18, wherein (1) said first substrate is physically positioned above said medium substrate and said connector, and (2) said medium substrate and said connector are physically positioned above said second substrate. In other words, the claimed connector is positioned between the first and second substrates. *Centola et al.* teach the opposite structure. As can be seen in FIG. 5 of *Centola et al.*, first and second substrates 105-1 and 105-2 are positioned between connectors 115-1, 115-2.

Withdrawal of the anticipatory rejection of claim 18 in view of the above is respectfully requested.

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With regard to Claim 19:

Claim 19 depends from claim 8, and is considered patentable at least for the reasons advanced with respect to claim 8.

In addition, the applied reference clearly fails to teach or disclose the invention of claim 19, wherein said first and second substrates are physically separated by a gap and said first and said chips are positioned within said gap. In other words, the claimed chips are positioned between the first and second substrates. *Centola et al.* teach the opposite structure. As can be seen in FIG. 4 of *Centola et al.*, first and second substrates 105-1 and 105-2 are positioned between chips 400 which are positioned on outer (uppermost and lowermost) surfaces of the substrates, respectively.

Withdrawal of the anticipatory rejection of claim 18 in view of the above is respectfully requested.

The 35 U.S.C. 103(a) rejection of claims 2-7, 9-13 and 16 as being unpatentable over *Centola et al.* (USPN 6,633,490) in view of *Lu et al.* (USPN 6,294,731) is traversed at least for the reasons advanced with respect to independent claims 1 and 8.

In addition, the Examiner's proposal to replace one of the *Centola et al.* connectors 115-1, 115-2 with the *Lu et al.* solder balls in order to connect the substrate 105-1 to the "external printed wiring board" 100 would render the connection between substrate 105-1 and "external printed wiring board" 100 permanent and would not be considered by a person of ordinary skill in the art because *Centola et al.* relate to the art of removably attaching a daughter board to a mother or backplane board. See Abstract, column 1, lines 10-38, and all figures of *Centola et al.* The obviousness rejection of claims 2 and 9 is therefore inappropriate for this additional reason.

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New claim 21 is patentable over the applied references at least for the reasons advanced with respect to independent claim 14.

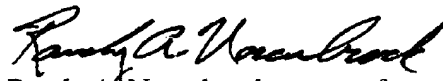
Each of the Examiner's rejections has been traversed. Accordingly, Applicants respectfully submit that all claims are now in condition for allowance. Early and favorable indication of allowance is courteously solicited.

The Examiner is invited to telephone the undersigned, Applicant's attorney of record, to facilitate advancement of the present application.

To the extent necessary, a petition for an extension of time under 37 C.F.R. 1.136 is hereby made. Please charge any shortage in fees due in connection with the filing of this paper, including extension of time fees, to Deposit Account 07-1337 and please credit any excess fees to such deposit account.

Respectfully submitted,

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